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Question Paper Code : 21176

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Third Semester

Electronics and Communication Engineering

EC 1201 — DIGITAL ELECTRONICS

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Implement the Ex-OR gate using NOR gate.
2. Find the complement of the function $F = \bar{x}y\bar{z} + \bar{x}\,\bar{y}z$.
3. Draw the inverter logic circuit using n-channel MOS devices.
4. What is totem-pole output?
5. What is encoder?
6. What is magnitude comparator?
7. Which flip flop is most suitable (manipulating excitation table easily) for the design of counter and which one is best for shift register design?
8. Distinguish between synchronous and asynchronous sequential circuits.
9. Enumerate the types of ROMs.
10. Compare PAL and PLA devices.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Using DeMorgan's theorem, convert the following Boolean expression to equivalent expression that has only OR and complement operations and also implement the function with only OR gates and inverters $F = \overline{xy} + \bar{x}z + \bar{y}z$. (8)

(ii) Simplify the Boolean function to a minimum number of literals using Boolean algebra and obtain its truth table.
$G = x\bar{y}z + \bar{x}\,\bar{y}z + \bar{w}xy + w\bar{x}y + wxy$. (8)

Or

(b) Simplify the function and implement with two-level NOR gate circuit $F(q,r,s,t) = \sum(5, 6, 9, 10)$.

12. (a) (i) Draw the RTL — NOR2 gate and explain its operation. (8)

(ii) Explain in detail the Emitter-Coupled Logic. (8)

Or

(b) (i) Write an elaborate note on Transistor-Transistor Logic. (8)

(ii) Draw the NAND gate and NOR gate using n-channel MOS device and explain its operation in detail. (8)

13. (a) Implement the following Boolean function with an 8 × 1 multiplexer. $F(A,B,C,D) = \sum(0, 3, 5, 6, 8, 9, 14, 15)$.

Or

(b) (i) Design the BCD to excess-3 code converter circuit using logic gates. (10)

(ii) A 3-bit message need to be transmitted together with an even parity bit. Design a 3-bit even parity generator circuit for this data transmission. (6)

14. (a) Design a counter with the following repeated binary sequence: 0, 1, 3, 5, 7 using T flip-flops. Treat the unused states as don't-care conditions.

Or

(b) Describe the shift register in detail.

15. (a) Discuss the programmable Logic Array (PLA) in detail.

Or

(b) Write an elaborate note on

(i) Static RAM cell. (8)

(ii) Field programmable Gate Arrays (FPGA). (8)

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